Differential Timing Methods for Circuit Emulation

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ITSF 2006
• What is Circuit Emulation and what is Differential Timing all about?
• Deployment Scenarios Examples
• Requirements
• Differential Timing Performance Results from our Lab
• Combined Differential Timing and Synchronous Ethernet Lab Results
CES Differential Timing

Reference ("Common") Clock

Recovered Service Clock

CES packets RTP 32 bit timestamp

Packet Switched Network

Clock Sink

IWF clock

Clock Source
CES Adaptive Timing

Recovered Service Clock

CES IWF

Clock Sink

E1

Packet Switched Network

CES packets
Packet Rate ~ Service Clock

Service Clock

Clock Source

IWF clock
Differential vs. Adaptive

• Differential Timing Pros:
  ▪ Handles well
    ▪ Packet Switched Network (PSN) impairments, and in particular Packet Delay Variation (PDV)
    ▪ Systematic PSN PDV due to beating effects
  ▪ Faster settling time compared to Adaptive
  ▪ Lower requirements for stability of IWF oscillator - leading to potentially cheaper solution with smaller footprint and power requirements

• Differential Timing Cons:
  ▪ Requires Common Reference Clock
TDM Transport
Synchronous First Mile

Metro / Access

First Mile
GPON

Customer
Premise

PRS

First Mile
DOCSIS

Customer
Premise

Metro
Ethernet

D
Circuit Emulation Inter-Working Function
Using Differential Timing
Synchronous Metro Ethernet

- **Metro / Access**
  - PRS

- **First Mile**
  - GPON

- **First Mile**
  - DOCSIS

- **Customer Premise**
  - E1
  - Clock Source

- **Customer Premise**
  - E1
  - Clock Sink

- **D** Circuit Emulation Inter-Working Function Using Differential Timing
Requirements

• Wander MTIE compliance as specified in G.8261
  ▪ consistent results across all
    • service clock frequencies
    • relevant common clock frequencies

• Robust to impairments introduced by
  ▪ packet switched network
  ▪ reference clock
  ▪ service clock

• Mid-range performance IWF oscillator and peripherals
TIE: Impairments

HP 53132A; Test: 66; FB3; Samples: 216007; Fast Sampling; Ref ch1: T1/Time Data Only; T1 1→2;

Holdover Frequency
offset < 12ppb

1.60 usec

800 nsec/div

10ms PDV
5% packet duplication
5% packet drop

Service Clock Disconnect

PSN disconnect

Remote Reference Disconnect (Short & Long)

PW Restart

Local Reference Disconnect (Short & Long)

T1, CC=10.24MHz, TCXO
MTIE: Impairments (first 5h)

G.824 Sync Intrf.  G.8261 case 1/2

T1, CC=10.24MHz, TCXO
MTIE: Service Clock Dependency

G.8261 case 1

G.823 Sync Intrf.

E1, CC=16.384MHz, TCXO

Brown  50ppm
Green   5ppm
Red     1ppm
Blue    0ppm

Magenta -1ppm
Cyan    -5 ppm
Yellow  -50ppm
TDEV: Service Clock Dependency

G.823 Sync Intrf.

E1, CC=16.384MHz, TCXO
Sync Ethernet Setup A

Reference Clock
Service Clock

ST2
10MHz
X2.5

Differential Timing
CES IWF
ETH PHY
25MHz Reference Clock

Fast Ethernet

CES

ETH PHY

CES IWF

E1
TDM Tester

Wander Measurement
MTIE: Sync Ethernet Results

G.8261 case 1

G.823 Sync Intrf.

PRELIMINARY RESULTS

Red PHYa Setup B
Blue PHYa Setup A

Magenta PHYb Setup A
Green PHYb Setup B
Black PHYb Setup B
TDEV: Sync Ethernet Results

Red  PHYa Setup B
Blue  PHYa Setup A
Green PHYb Setup B
Black PHYb Setup B
Magenta PHYb Setup A

G.823 Sync Intrf.
Conclusions

• Packet switched networks which provide common reference clock are happening now

• Differential timing is compliant with strictest performance requirements

• Differential timing is a robust and cost effective solution
Thank You