Improving Synchronization Standards

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Agenda

- Synchronization standards from user perspective
- Synchronous Ethernet G.8262
- Proposal for simple improvements G.8262+
  - Long term phase transients (holdover)
  - Short term phase transients
Synchronization standards

- Objective of standards is to clearly state what is needed, and not necessarily why it is needed.
- Standard is written by consensus between standard participants so requirements may not always be the most optimum solution—standard requirements are quite often compromise between conflicting interests.
- Telecom synchronization standards are built on 50 year synchronization history—Many standard requirements have long history for backward compatibility.
Synchronous Ethernet

- Synchronous Ethernet ITU-T G.8262 is closely based on SDH Equipment Clock ITU-T G.813 standard (almost carbon copy)-Why fix something which is not broken
- There are few requirements in G.8262 which are carried forward from old standard and which may not represent reality in the field.
  - Long term phase transients (holdover)
  - Short term phase transients

G.813 has many other dependencies but for the purpose of this presentation only relevant ones are shown

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Long term phase transients
Synchronizer constantly calculates the average frequency of the reference it is locked to, so that if the reference fails and none of the other references is available, the synchronizer goes into holdover mode where it generates output clock based on calculated average value. Holdover stability depends on resolution of the synchronizer averaging algorithm and on frequency stability of the oscillator used as synchronizer master clock.

![Diagram of PLL with Holdover](image)

- **Input frequency**
- **Output frequency**

- **Initial Holdover Limit**
- **Input line gets cut**
  (input reference frequency Goes to zero)

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Long term phase transient (Holdover) Cont.

\[ DT(S) = \{(a_1 + a_2) S + 0.5 b S^2 + c\} \text{ [ns]} \]

where:

- \( a_1 = 50 \text{ ns/s} \) (see Note 1);
- \( a_2 = 2000 \text{ ns/s} \) (see Note 2);
- \( b = 1.16 \times 10^{-4} \text{ ns/s}^2 \) (see Note 3);
- \( c = 120 \text{ ns} \) (see Note 4).

NOTE 1 – The frequency offset \( a_1 \) represents an initial frequency offset corresponding to \( 5 \times 10^{-8} \) (0.05 ppm).

NOTE 2 – The frequency offset \( a_2 \) accounts for temperature variations after the clock went into holdover and corresponds to \( 2 \times 10^{-6} \) (2 ppm). If there are no temperature variations, the term \( a^2S \) should not contribute to the phase error.

NOTE 3 – The drift \( b \) is caused by ageing: \( 1.16 \times 10^{-4} \text{ ns/s}^2 \) corresponds to a frequency drift of \( 1 \times 10^{-8} \text{/day} \) (0.01 ppm/day). This value is derived from typical ageing characteristics after 10 days of continuous operation. It is not intended to measure this value on a per day basis, as the temperature effect will dominate.

NOTE 4 – The phase offset \( c \) takes care of any additional phase shift that may arise during the transition at the entry of the holdover state.
Common holdover implementation

**PLL**
- Phase Detector
- Loop Filter
- Voltage Controlled Oscillator

**Hybrid PLL**
- Phase Detector
- Voltage Controlled Crystal Oscillator
- DAC
- VCXO

**Digital PLL**
- Phase Detector
- Digitally Controlled Oscillator

Crystal Oscillator

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Common holdover implementation Cont.

- For VCXO (OCVCXO) with +/-20ppm range and 10 bit DAC resolution is 40ppm/1024 = 39ppb
- Holdover accuracy is than +/-19.5ppb
- When you add margin for inherent DAC inaccuracies you get to +/-50ppb
- With 16 bit DAC (very common today) one could get accuracy of +/-0.3ppb
Frequency generated by DCO is:

Where:
- control word from low pass filter
- frequency of crystal oscillator
- size of accumulator in bits

For 24 bit accumulator (high end in late 80s) step size is —

Holdover accuracy is than +/-28ppb

Nowadays accumulators with 32, 48 and 64 bit are used. For example 32 bit accumulator provide better than 0.2ppb accuracy
During the last 15 years all MSCC Network Timing devices and devices from other vendors have initial holdover accuracy better than 0.5ppb.
Short term phase transients
During the reference rearrangements (reference switch), output phase should not experience sudden phase movement regardless of the phase offset between references.
Short term phase transients (G.8262) Cont.
Handling of short term phase transients

Digital PLL

- **Phase Detector**
- **Digitally Controlled Oscillator (DCO)**
- **TIE Comp.**

Inputs: in0, in1
Outputs: out

Active reference
Redundant reference
Output

- PLL locked to Ref0
- PLL locked to Ref1

Compensated in TIE block
This requirement goes back to 80s (T1.101). At that time all synchronization solutions were made from discrete components (off the shelf logic) and clock frequencies were typically 10MHz and lower.

For the last 15 years all MSCC (formerly Zarlink) Network PLLs, and PLLs from other vendors have phase transient of sub 10ns and quite often sub 1ns (at least 100 times below the standard limit!)

It is similar for custom (FPGA) solutions because internal sampling clock is at least 100MHz.
### Who could benefit from the change

<table>
<thead>
<tr>
<th>Application</th>
<th>Frequency (ppb)</th>
<th>Phase (µs)</th>
<th>Time (µs)</th>
<th>Reference Document</th>
</tr>
</thead>
<tbody>
<tr>
<td>CDMA</td>
<td>±50</td>
<td></td>
<td>±3</td>
<td>TIA/EIA-95-B [53]</td>
</tr>
<tr>
<td>CDMA2000</td>
<td>±50</td>
<td>±10 (&gt;8hrs) when external timing source disconnected</td>
<td></td>
<td>3GPP2</td>
</tr>
<tr>
<td></td>
<td></td>
<td>±3 (Traceable &amp; Synchronous to UTC)</td>
<td></td>
<td>C.S0002-E v2.0 [54]</td>
</tr>
<tr>
<td>GSM</td>
<td>±50</td>
<td></td>
<td></td>
<td>ETSI</td>
</tr>
<tr>
<td></td>
<td>±100 (pico BS)</td>
<td></td>
<td></td>
<td>TS 145.010 [54]</td>
</tr>
<tr>
<td>UMTS-FDD (WCDMA)</td>
<td>±50 (Wide area BS)</td>
<td>12.8 (MBSFN-3GPP Release 7/8)</td>
<td></td>
<td>3GPP</td>
</tr>
<tr>
<td></td>
<td>±100 (Medium range BS)</td>
<td></td>
<td></td>
<td>Frequency: TS 25.104 [64]</td>
</tr>
<tr>
<td></td>
<td>±100 (Local area BS)</td>
<td></td>
<td></td>
<td>MBSFN: TS 25.346 [66]</td>
</tr>
<tr>
<td></td>
<td>±250 (Home BS)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>UMTS-TDD (WCDMA)</td>
<td>±50 (Wide area)</td>
<td>±2.5</td>
<td>±1 (between Macro eNB and Home eNB)</td>
<td>3GPP</td>
</tr>
<tr>
<td></td>
<td>±100 (Local area)</td>
<td></td>
<td></td>
<td>Frequency: TS 25.105 [65]</td>
</tr>
<tr>
<td></td>
<td>±250 (Home eNB)</td>
<td></td>
<td></td>
<td>Phase: TS 25.402 [67]</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Home eNB: TR 25.866 [69]</td>
</tr>
<tr>
<td>TD-SCDMA</td>
<td>±50</td>
<td>±3</td>
<td></td>
<td>3GPP</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>TS 25.123[63]</td>
</tr>
<tr>
<td>LTE (FDD)</td>
<td>±50 (Wide area)</td>
<td>CDMA handover and Synchronized E-UTRAN GPS time</td>
<td>≤ 3 (small cell)</td>
<td>3GPP</td>
</tr>
<tr>
<td></td>
<td>±100 (Local area)</td>
<td></td>
<td>≤ 10 (large cell)</td>
<td>Frequency: TS 36.104 [72]</td>
</tr>
<tr>
<td></td>
<td>±250 (Home eNB)</td>
<td></td>
<td></td>
<td>Time: TS 36.133 [73]</td>
</tr>
<tr>
<td>LTE (TDD)</td>
<td>±50</td>
<td>≤ 3 (small cell)</td>
<td></td>
<td>3GPP</td>
</tr>
<tr>
<td></td>
<td></td>
<td>≤ 10 (large cell)</td>
<td></td>
<td>Frequency: TR36.922 [75]</td>
</tr>
<tr>
<td></td>
<td></td>
<td>CDMA handover and Synchronized E-UTRAN:</td>
<td></td>
<td>Phase &amp; Time: TS36.133 [73]</td>
</tr>
<tr>
<td></td>
<td></td>
<td>≤10 (&gt;8hours) when external timing source disconnected</td>
<td></td>
<td></td>
</tr>
<tr>
<td>LTE-A</td>
<td>±50 (Wide area)</td>
<td>≤ ±1.5 or lower, depending on service</td>
<td></td>
<td>Summarized in MBH IA Ph3 Sync TimePhase</td>
</tr>
<tr>
<td></td>
<td>±100 (Local area)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>±250 (Home eNB)</td>
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Network PLLs in field have more than 100 times better short term stability than requested by G.8262 standard.

Network PLLs in field have more than 100 times better initial holdover accuracy than requested by G.8262 standard.

New variant of G.8262 could be generated (G.8262+) to add these changes.

Majority of equipment in the field would be compatible to this standard.

These changes would reduce requirement for synchronization devices in base stations and it would simplify IEEE1588 slave devices where IEEE1588 is used in tandem with Synchronous Ethernet.
End