CSAC Design Services

Introduction
Accelerate your design processes to take advantage of the performance enhancing Chip Scale Atomic Clock CSAC technology with Chronos' CSAC Design Services

Fundamental research and product realisation has been on-going with regard to Chip Scale Atomic Clock (CSAC) technology at the National Institute of Standards and Technology (NIST) and Symmetricom for over 10 years[1,2]. CSAC is arguably the biggest leap forward in oscillator stability, size, and power consumption performance in the last 35 years. With a frequency stability comparable to today's low cost Rubidium (Rb) atomic frequency standards, but at only 5% of the power consumption, CSAC is the ideal candidate for new tactical designs where holdover performance together with low power consumption and small form factor are critical to your product requirements.

Early adopters need to accelerate their design process to take advantage of this performance enhancing technology. This datasheet serves to explain how Chronos Technology Ltd (CTL) can use our 25 years experience in phase locked loop (PLL) design, oscillator integration and system testing to assist early adopters to accelerate CSAC implementation.

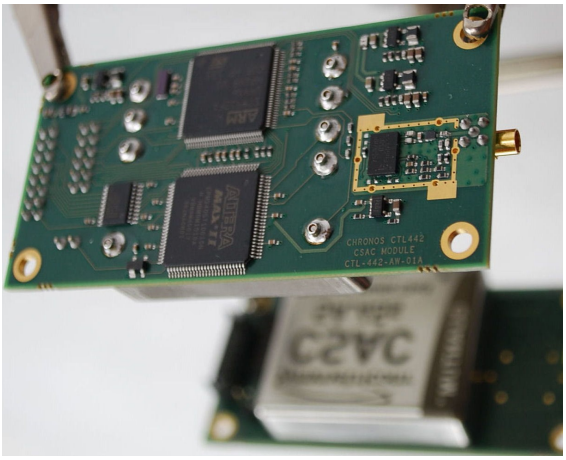
Disciplining Oscillators
High specification/quality oscillators are generally not designed into complex equipment to only ever operate in free run mode. Commonly they are disciplined by a source of better timing stability e.g. GPS and their capabilities are used to improve the medium term variation in the timing signal (wander).

This, for many applications such as portable radio or RF emitter systems, is likely to be the case for CSAC which will be designed into a PLL or have its drift corrected using a numerically controlled oscillator (NCO). Key characteristics must be analysed to ensure the PLL or NCO design is optimised. These include performance under varying environmental conditions, particularly temperature, the granularity of the oscillator control, and hold-over performance in the event of loss of the disciplining source.

Design Process
Chronos has provided design services and consultancy to many of our customers in the areas of oscillator integration, system design and test. Our stepwise approach means that we will understand the application and if the CSAC will be of benefit, then work to enable the most cost effective implementation strategy.

Our design service process is flexible to allow rapid development and prototyping but also formal enough using a gate methodology to ensure that requirements are captured and met. The Product Requirement Document (PRD) is generated early in this process which will form the basis the design work.

The PRD defines the scope of the project deliverable including test plan e.g. tested reference design for customer fabrication, OEM PCB or finished unit for system integration. Testing will normally be carried out in CTL labs and assistance can be provided for the customer to mirror tests in an integrated environment.



Chronos Chip Scale Design Board—CTL 442

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CSAC Design Services

Discover Design Develop Deliver

Pedigree

Chronos' pedigree in the design and delivery of integrated systems spans 25 years, with specific additional expertise in the testing of timing and synchronisation systems playing a major role in our business. For example, our Time Interval Error (TIE) testing capability enables nanosecond granularity time error analysis over very long observation periods extending over months and years if required. Testing can be performed in both constant and variable temperature environments, against UTC calibrated time references such as Cesium (Cs) atomic standards and GPS receivers with Rubidium disciplined oscillators.

The testing capabilities include industry standard test equipment and test software, including the use of Chronos' SyncWatch measurement system for real time 24 x 7 monitoring via web enabled reporting and results dissemination if required.

Other testing includes environmental, vibration and shock. This may be carried out at Chronos' facility or approved sub-contractors or at the customers facility. Results of vibration and shock testing on the CSAC component are documented by Symmetricom[3,4,5].

Chronos time and timing standards are continuously compared to UTC-GPS and have been calibrated to UTC-NPL the UK's national time standard run by the National Physical Laboratory at Teddington, Middlesex. NPL certification can be obtained for specific designs if required.

Manufacturing Options

Once the design has been approved and proven, Chronos can take charge of product manufacture and hand over finished goods or a reference design and critical components i.e. CSAC and GPS silicon are supplied for the customer to manufacture using their own facilities/services. Either way the customer can be assured of meeting the goals of designing with CSAC to achieve significant technological breakthrough with this emerging technology.

CSAC Development Board

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